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PERSONAL SUMMARY

Embedded Systems MSc student with a strong academic foundation in Computer and System Architecture, hardware software co-design, and full software stacks. Proficient in Python, C, and Computer Architecture, with hands-on experience in system performance analysis, workload modelling, and FPGA-based design on Arm Cortex platforms. Skilled in Verilog, MATLAB, and embedded firmware development.

WORK EXPERIENCE

Apitronix Semiconductor Ltd., **York; Microelectronics Engineer Intern** **June 2026 – Present**

- Contributing to pre-silicon development of a safety-critical dual-core RISC-V (RV32I, Hazard3) processor, prototyping and characterising a custom on-chip ADC.
- Brought up the Hazard3 soft-core SoC on a Lattice ECP5 FPGA, integrating the CPU with the clock/timer/GPIO (CTIO) peripheral and establishing a full JTAG program-and-debug flow via OpenOCD and GDB.
- Implemented a time-based ADC from discrete components (resistor, capacitor, hysteresis-free comparator), using the RC charge curve and CTIO input-capture timing to convert analog voltages to digital.
- Wrote bare-metal RISC-V firmware in Embedded C to drive the ADC, capture timing, and linearise its response with calibrated lookup tables.
- Designed a two-channel CANPico's physical-layer PCB in KiCad (dual TCAN6062V-Q1 transceivers) with switchable bus termination, TXD isolation, and standby-strap options — as a daughterboard mating to the ECP5 evaluation board's Versa headers.

National Manufacturing Institute (NMIS), **Glasgow; Software Intern** **June 2024 – September 2024**

- Developed a custom Behaviour Tree GUI using Python and PyQt to streamline cobot task management in manufacturing environments.
- Engineered synchronous and asynchronous logic for handling concurrent tasks, enhancing operational flexibility.
- Introduced SVG support to enable high-quality visuals and scalable graphics, improving the overall user experience.
- Collaborated cross-functionally with hardware and robotics engineers, using Git for version control and code review, to align software solutions with real-world manufacturing requirements.

EDUCATION & QUALIFICATIONS

University of Leeds, **MSc. (Eng) Embedded Systems Engineering** **September 2025 – Present**

- Modules: Control Systems Design, Digital Signal Processing, FPGA Design for System-on-Chip, Embedded Microprocessor System Design, Medical Electronics and E-Health.
- Developing advanced proficiency in RTOS, Embedded C, Verilog, and MATLAB for complex system programming, modelling, and performance simulation on Arm-based platforms.

University of Edinburgh, **(BHons.) Electronics & Computer Science** **September 2021 – July2025**

- Modules include Computer Architecture, Quantum Electronics, Digital Systems Design, Analog Data Structure, Software & Embedded Systems.
- Dissertation: "Comparing Recursive Queries on Relational and Graph Database Systems" – Conducted comparative performance analysis between MySQL and Neo4j; authored a Recursive Descent Parser in Python to interpret organisational data structures programmatically.

Delhi Public School (DPS–MIS), **Doha, Qatar** **April 2016 – March 2021**

- CBSE Boards (India): Class 10 – 91.6%, Class 12 – 94.0%; awarded the Scholar Badge for academic excellence.
- Higher grades in Mathematics (B), English (A), Physics (A), Chemistry (A), Physical Education (A).
- Represented DPS–MIS at the CBSE National Swimming Championship (under 17), 2018–2019.

TRAINING & PROJECTS

NLOS SDR Bare-Metal Transceiver with Custom DSP, *GitHub* **February 2026 – May 2026**

- Developed a bare-metal custom library on the Altera DE1-SoC, targeting the Cyclone V FPGA fused with a DualCore Arm Cortex-A9 HPS, to implement a Non-Line-of-Sight (NLOS) communication system.
- Implemented custom FIR (low-pass and band-pass) and FFT filtering chains in Embedded C to process SDR audio inputs and improve signal recovery.
- Benchmarked the FFT filtering chain on 8,192 complex I/Q samples, reducing execution time from 671 ms (scalar C baseline) to 72 ms via NEON SIMD with precomputed lookup tables — a 9.3x speedup (~89% reduction) with no loss of accuracy.

Hardware-Accelerated Pre-Trade Risk Filter, *GitHub* **February 2026– April 2026**

- Architected an ultra-low latency pre-trade risk engine on the Cyclone V FPGA to autonomously intercept fat finger errors and compliance breaches.
- Engineered a custom Verilog data path evaluating 10 simultaneous stateful risk rules, including price deviation, long/short position limits, and message throttling.
- Achieved end-to-end trade validation across all 10 risk rules in just 20 ns per transaction, demonstrating deterministic ultra-low-latency performance suitable for high-frequency trading environments.

Digital Systems Laboratory – Custom Processor Design on FPGA, *UoE* **January 2025 – April 2025**

- Implemented a processor on an FPGA using Verilog over 3 progressive project phases.
- Developed a full VGA display subsystem, including a frame buffer, dual-port video memory, and VGA signal generator with accurate synchronization and raster scanning.
- Collaborated within a small team to integrate processor, memory, VGA, and optional peripherals, with sole responsibility for VGA and IR subsystems.

EXTRA-CURRICULAR EXPERIENCE

Vice President, EUIS, *University of Edinburgh,* UK **September 2023 – May 2024**

- Lead & coordinated a wide range of club events, fostering a vibrant and inclusive community for students.
- Provided strategic direction to the executive team, ensuring successful execution of club initiatives.
- Maintained constant communication with club members, and external collaborators to promote events seamlessly.

SKILLS & INTERESTS

- **Programming Languages:** Python, C, C++, Java, Haskell, Verilog, SQL, Go, Bash / Shell Scripting, Cypher
- **Tools & Software:** MATLAB, VS Code, PyQt, LTspice, KiCAD, STM32CubeIDE, Quartus Prime, Neo4j
- **Version Control:** Git, GitHub

CERTIFICATIONS

- Embedded Systems Programming on ARM Cortex-M3/M4 Processor, Udemy (December 2025)